DEVICE AND METHOD FOR PROTECTING GATE TERMINAL AND LEAD

BACKGROUND

1. Field of the Invention

[0001] The present invention generally relates to a device and method for protecting gate terminal and lead, and more particularly to a device and method for protecting gate terminal and lead at stage of scribing and spalling.

2. Description of the Prior Art

[0002] In fabrication of thin film transistor (TFT) liquid crystal display (LCD) device, an array substrate and a color filter substrate are provided respectively, in which thin film transistor array on the array substrate are formed by thin film deposition, lithographic process, and etching step of semiconductor process. Having been formed the two substrates, an assembling process, a scribing step, and a spalling step are performed. The scribing and spalling steps are to remove peripheral regions on the color filter substrate such that contact plugs of gate terminals on the array substrate can be exposed.

[0003] The scribing and spalling steps can be shown in Figure 1, wherein a display region on an array substrate 100 includes a thin film transistor and a peripheral region includes a gate line 102. The thin film transistor, covered and protected by a passivation layer 112, has a gate 102, gate insulating layer 104, island semiconductor layer 106, and source/drain 108. A contact plug 114 on gate terminal of the gate line 102 is used to connect driver IC electrically. Another substrate 130, which is also called color filter substrate, has a black matrix on the inner side and assembled with the array substrate 100. In the TFT-LCD fabricating process, after the two substrates are assembled, the scribing and spalling steps are performed. In Figure 1, scribing line is denoted by dash line, and the contact plug 114 is exposed after scribing.

[0004] However, material of the gate insulating layer 104 and the passivation layer 112 is silicon nitride, which has less strain at the stage of scribing and spalling steps to break the two layers. Further, after the gate insulating layer 104 and the passivation layer 112 are broken, gas or origin of pollution will reach the gate line 102 along splits to make the gate terminal of gate line 102 corrosion or oxidation. This will cause the display panel fail. Therefore, a solution for resolving issues caused at the scribing and spalling steps is necessary.

SUMMARY

[0005] In accordance with the present invention, a resist region between the passivation and the gate insulating layer on the array substrate is provided. When the panel is scribed and spalled, the resist region can provide sufficient strain to protect the gate insulating layer and passivation layer from breaking.

[0006] It is another object of this invention to provide a less activity resist region compared to the gate terminal and lead of gate line to prevent gate line from corrosion.

[0007] It is a further object of this invention to have a floating resist region such that there is no electrical connection between the resist region and any circuit of the display panel.

[0008] It is still another object of this invention that formation of the resist region can be combined to the present TFT fabrication process without increasing TFT fabrication cycle time.

[0009] In one embodiment, a device for protecting a gate terminal and lead at stage of scribing and spalling a LCD panel is provided, wherein the LCD panel comprises a first substrate with thin film transistor array thereon and a second substrate thereon within color filter opposite to the thin film transistor array. The device comprises a resist region covering the gate terminal and lead of the gate electrode line and between a passivation layer and a gate insulating layer, and located at a scribing line on margin of the second substrate of the panel, thereby the resist region can protect the passivation layer, and the gate insulating layer

from cracking, the gate terminal and lead from corrosion after a portion of the second substrate is removed along the scribing line.

[0010] A method for protecting a gate terminal and lead at stage of scribing and spalling a LCD panel is also provided. The method comprises steps of forming the gate electrode and the gate electrode line on a first substrate, wherein the first substrate is also called array substrate or lower substrate, and the gate electrode line comprises the gate terminal and the lead. Then, a blanket gate insulating layer is deposited on the gate electrode, the gate electrode line, and the substrate. Next, an island semiconductor layer is formed on the gate electrode and a source electrode and a drain electrode on the island semiconductor layer, and a resist region is simultaneously formed on the gate insulating layer and covering the gate terminal and the lead of a gate electrode line, wherein the resist region is located at a scribing line on margin of a second substrate with color filter thereon. Afterward, a blanket passivation layer is deposited on the source electrode, the drain electrode, and the resist region thereby the resist region can protect the passivation layer, and the gate insulating layer from cracking, the gate terminal and the lead from corrosion after a portion of the second substrate is removed along the scribing line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0012] Figure 1 illustrates a schematic representation of an LCD panel at the stage of scribing and spalling by using conventional method wherein passivation layer, gate insulating layer, gate terminal as well as lead of gate line on array substrate may be damaged;

[0013] Figure 2 illustrates a schematic representation of a method in accordance with this invention wherein gate electrode and gate line are formed on an array substrate with a gate insulating layer thereon;

[0014] Figure 3 illustrates a schematic representation of a method in accordance with this invention wherein a thin film transistor is formed on the array substrate and a resist region is formed on the gate insulating layer;

[0015] Figure 4 illustrates a schematic representation of a method in accordance with this invention wherein a passivation layer is formed on the thin film transistor and a contact window is formed on the gate terminal;

[0016] Figure 5 illustrates a schematic representation of a method in accordance with this invention wherein the resist layer can protect passivation layer, gate insulating layer, and gate terminal as well as lead of gate line on the array substrate at the stage of scribing and spalling; and

[0017] Figure 6 illustrates a top view of the resist region on the gate terminal and lead in accordance with this invention.

DETAILED DESCRIPTION

[0018] Some sample embodiments of the present invention will now be described in greater detail. Nevertheless, it should be recognized that the present invention can be practiced in a wide range of other embodiments besides those explicitly described, and the scope of the present invention is expressly not limited except as specified in the accompanying claims.

[0019] This invention provides a device for protecting a gate terminal and lead at stage of scribing and spalling a LCD panel, wherein the LCD panel comprises a first substrate with thin film transistor array thereon and a second substrate thereon within color filter opposite to the thin film transistor array. The device comprises a resist region covering the gate terminal and lead of gate electrode line and between a passivation layer and a gate insulating layer, and located at a scribing line on margin of the second substrate of the panel, thereby the resist region can protect the passivation layer and the gate insulating layer from

cracking, the gate terminal and lead from corrosion after a portion of the second substrate is removed along the scribing line. Material of the resist region is metal and the resist region is floating between the gate insulating layer and the passivation layer. Activity of the resist region is less than the gate electrode line.

[0020] Distance between the scribing line and margin of the resist region is about more than 50 μm, and width of the resist region is larger than the gate terminal and the gate electrode line.

[0021] Material of the resist region can be the same as source/drain electrodes of the thin film transistor, and step of formation the resist region is at a step of formation of the source/drain electrodes, wherein formation of the resist region comprises steps of providing the first substrate with a gate electrode and the gate electrode line thereon, and the gate insulating layer covering the gate electrode, the gate electrode line, and the array substrate, wherein the first substrate is also called array substrate or lower substrate. Then, an island semiconductor layer is formed on the gate insulating layer and over the gate electrode. Next, a blanket metal layer is deposited on the island semiconductor layer and the gate insulating layer. A lithographic process is then performed to the conductive layer by using a reticle with a source pattern and a drain pattern on the gate electrode and a resist region pattern on the gate terminal and lead. Afterward, the conductive layer is etched to form the source/drain electrodes and the resist region.

[0022] Material of the resist region can be the same as island semiconductor layer of the thin film transistor, and step of formation the resist region is at the step of formation of the island semiconductor layer, wherein formation of the resist region comprises steps of providing the first substrate with a gate electrode and the gate electrode line thereon, the gate insulating layer blanket on the gate electrode, the gate electrode line wherein the first substrate is also called array substrate or lower substrate, and the array substrate. Then, a blanket semiconductor layer is deposited on the gate insulating layer. Next, a lithographic process is performed to the semiconductor layer by using a reticle with an island pattern on the gate electrode and a resist region pattern on the gate terminal and the lead. Afterward,

the semiconductor layer is etched to form the island semiconductor layer and the resist region.

[0023] This invention also provides a method for protecting a gate terminal and lead at stage of scribing and spalling a LCD panel. The method comprises steps of forming the gate electrode and the gate electrode line on a first substrate, wherein the first substrate is also called array substrate or lower substrate, and the gate electrode line comprises the gate terminal and the lead. Then, a blanket gate insulating layer is deposited on the gate electrode, the gate electrode line, and the substrate. Next, an island semiconductor layer is formed on the gate electrode and a source electrode and a drain electrode on the island semiconductor layer, and a resist region is simultaneously formed on the gate insulating layer and covering the gate terminal and the lead of the gate electrode line, wherein the resist region is located at a scribing line on margin of a second substrate with color filter thereon. Material of the resist region is metal and the resist region is floating between the gate insulating layer and the passivation layer. Activity of the resist region is less than the gate electrode line. Distance between the scribing line and margin of the resist region is about more than 50 um, and width of the resist region is larger than the gate terminal and the gate electrode line. Afterward, a blanket passivation layer is deposited on the source electrode, the drain electrode, and the resist region thereby the resist region can protect the passivation layer and the gate insulating layer from cracking, the gate terminal and the lead from corrosion after a portion of the second substrate is removed along the scribing line.

[0024] Material of the resist region can be the same as source/drain electrodes of the thin film transistor, and step of formation the resist region is at a step of formation of the source/drain electrodes. Formation of the resist region comprises steps of forming an island semiconductor layer on the gate insulating layer and over the gate electrode. Then, a blanket metal layer is deposited on the island semiconductor layer and the gate insulating layer. Next, a lithographic process is performed to the conductive layer by using a reticle with a source pattern and a

drain pattern on the gate electrode and a resist region pattern on the gate terminal and the lead. Afterward, the conductive layer is etched to form the source electrode, the drain electrode and the floating metal resist region.

[0025] One embodiment is disclosed according to this invention. Referring to Figure 2, a gate electrode 12 (at right hand side display region) and a gate line 12(at left hand side display region) are formed on a first substrate 10, and a blanket gate insulating layer 14 is formed on the gate electrode 12, gate line 12, and first substrate. The first substrate 10 is also called array substrate or lower substrate of LCD panel. When a back light source is used as light source for liquid crystal display device, the first substrate 10 is transparent, such as glass or transparent plastic. When a front light source is used as light source of the display device, the first substrate 10 should not necessary be transparent. Material of the gate electrode layer 12 can be metal or any kind of conductive material, such as aluminum or aluminum alloy, molybdenum or molybdenum tungsten alloy, chromium or tantalum. Formation of the gate electrode layer 12 is to deposit a conductive layer by using sputtering method on the first substrate 10, and lithographic and etching processes are performed to form a gate electrode pattern on a predetermined position. When gate electrode pattern is formed on the first substrate 10, gate line 12 is also formed on the first substrate 10. The gate line 12 includes gate terminal and lead, which always at one margin of the display panel. The gate line and gate electrode 12 are formed at one step and have the same material.

[0026] A blanket insulating layer 14 is formed on the first substrate 10 to cover the gate electrode and the gate line 12. The insulating layer 14, also called gate insulating layer, material of which is silicon nitride, is a blanket deposited on the gate electrode and the gate line 12 and first substrate 10. The insulating layer 14 serves as the gate dielectric layer of the thin film transistor and provides insulate isolation on the other area. Formation of the insulating layer 14 uses popular chemical vapor deposition method.

[0027] Referring to Figure 3, a thin film transistor is formed on display region and a resist region 20 is formed on the peripheral region. Formation of the thin film transistor is to form the island semiconductor layer 16 and metal source/drain 18. Material of the resist region 20 may be the same as metal source/drain 18, island semiconductor 16, or a composite layer including both semiconductor layer and metal layer. Position of the resist region 20 is about on scribing line when the display panel is assembled and scribed, in which distance between the scribing line and both ends of the resist region 20 is about more than 50 μm, and width of the resist region is larger than the gate terminal and lead. Activity of preferred material of the resist region 20 is less than the gate line 12, because the gate line 12 will be corroded or oxidized after the resist region 20 is completely eroded or oxidized when both the passivation layer 22 and the gate insulating layer 14 are crack. The less activity of the resist region 20 is the longer duration of resist region 20 is eroded or oxidized, and possibility of gate line 12 eroding or oxidizing can be decreased. The resist region 20 is floating between the passivation layer 22 and the gate insulating layer 14 and do not connect electrically with other conductivity or semiconductor.

[0028] Formation of the resist region 20 can have many ways. One method is to use material of metal source/drain 18 for the resist region 20. The method is to form an island semiconductor layer 16 on the insulating layer 14 and over the gate electrode layer 12. The semiconductor layer 16 primarily provides a channel region of the thin film transistor. In thin film transistor-liquid crystal display device, channel region is above the gate electrode layer 12, and also named back channel region. The semiconductor layer 16 uses a composite layer within double layers, which is underneath amorphous silicon layer and upper n-doped amorphous silicon layer. The underneath amorphous silicon layer provides channel region of the transistor, while the upper n-doped amorphous silicon layer serves as ohmic contact between metal and semiconductor to reduce resistance between metal source/drain and semiconductor layer.

[0029] A conductive layer 18, served as source and drain electrodes, are formed on the island semiconductor layer 16, and a thin film transistor is therefore formed. Material of this conductive layer 18 can be aluminum or aluminum alloy, molybdenum or molybdenum tungsten alloy, chromium or tantalum. Formation of the source and drain electrodes is to deposit a blanket conductive layer on the island semiconductor layer 16 and the gate insulating layer 14, and then a lithographic process is performed to remove a portion of conductive layer 18 to leave the source and drain electrodes. In this lithographic process, there is a resist pattern on peripheral of the reticle, and the resist region 20 is formed after the following etching step.

[0030] Another method is to form the resist region 20 simultaneously when the island semiconductor layer 16 is formed. The method is to form a blanket semiconductor layer on the gate insulating layer 14. Then, a lithographic process and an etching step are performed to form an island semiconductor layer 16 over the gate electrode 12. In this lithographic process, there is a resist pattern on peripheral of the reticle, and the resist region 20 is formed after the etching step.

[0031] A further method is to comply with the current 4 lithographic processes, which means formation of the island semiconductor layer and the source/drain utilize one lithographic process. A blanket semiconductor layer and a blanket metal layer are deposited sequentially on the gate insulating layer 14. Then, a lithographic process and an etching step are performed to form an island semiconductor layer 16 over the gate electrode 12 and a metal source/drain 18 thereon. In this lithographic process, there is a resist pattern on peripheral of the reticle, and the resist region 20 is formed after the etching step.

[0032] Referring to Figure 4, a blanket passivation layer 22 is formed on the thin film transistor, the resist region 20 and the gate insulating layer 14. The passivation layer 22 can be silicon nitride and formed by chemical vapor deposition method. Then, another lithographic process and an etching step are performed to form contact windows for drain electrode and the terminals on the peripheral of display panel. The contact plug 24 in Figure 4 uses transparent

conductive layer, and formation of the contact plug 24 can be combined to formation of the transparent conductive electrode. After the passivation layer 22 is formed, the resist region 20 is floating.

[0033] Referring to Figure 5, a second substrate 30, which is also called color filter substrate, is assembled to the array substrate 10 and scribed and spalled, wherein the dash line indicates scribing line. Inner side of the color substrate 30 has a black matrix 32 opposite to the array in the figure. When the color filter substrate 30 is cut along the scribing line to remove the peripheral region, the resist region 20 provides sufficient stress for array substrate 10 to protect passivation layer 22 and gate insulating layer 14 from cracking. Even if the passivation layer 22 and gate insulating layer 14 is broken, eroding or oxidizing rate of the gate line 12 can be postponed due to activity of the resist region 20 is less than the gate line 12. After the scribing and spalling steps, contact plug 24 on the gate terminal is exposed, and will connect to driver IC on flexible printed circuit board electrically.

[0034] Referring to Figure 6, a top view of the resist region 20 is shown. Width of the resist region 20 is larger than gate terminal and lead, and distance between the scribing line and both ends of the resist region 20 is about more than 50 μm. Such kind of dimension will provide better strain.

[0035] This invention provides a resist region between the passivation and the gate insulating layer on the array substrate. When the panel is scribed and spalled, the resist region can provide sufficient strain to protect the gate insulating layer and passivation layer from breaking. Moreover, this invention provides a less activity of the resist region compared to the gate terminal and lead of gate line to prevent gate line from corrosion or oxidization, and has a floating resist region such that there is no electrical connection between the resist region and any circuit of the display panel. Further, formation of the resist region can be combined to the present TFT fabrication process without increasing TFT fabrication cycle time.

[0036] Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.

[0037] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.